



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/615,605 | 07/13/2000 | Iwao Higashikawa | 04329.2348 | 4718 |

22852 7590 03/13/2003

FINNEGAN, HENDERSON, FARABOW, GARRETT &
DUNNER LLP
1300 I STREET, NW
WASHINGTON, DC 20006

[REDACTED] EXAMINER

NGUYEN, MICHELLE P

| ART UNIT | PAPER NUMBER |
|----------|--------------|
| 2851 | |

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-----------------------------|-------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 09/615,605 | HIGASHIKAWA, IWAO | |
| | Examiner Michelle Nguyen | Art Unit 2851 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____ .
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-20 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 13 July 2000 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1.) Certified copies of the priority documents have been received.
 2.) Certified copies of the priority documents have been received in Application No. _____ .
 3.) Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>4</u> . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 9-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the mask arranging position" in lines 14-15. There is insufficient antecedent basis for this limitation in the claim. Further, in line 16, "position measuring mark" should be --position measuring marks--.

Claims 11-17 include all limitations set forth in claim 9.

Claim 12 recites the limitation "said defect comprises a defect that lowers the reflectivity and a reflection defect" in lines 7-8. It is not understood with respect to what the first defect lowers the reflectivity. Further, it is not understood to what type of defect the reflection defect refers.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-10 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,015,866 to Hayashi.

With regard to claim 1, Hayashi discloses a pattern forming method in which a desired pattern (pattern area PA) is exposed on to a surface a substrate (wafer W), comprising the steps of:

detecting a lateral deviation amount of the wafer W (see Col. 7, lines 43-7, Col. 9, lines 8-14, Fig. 1);

analyzing the mutual positional relationship between the detected lateral deviation amount and the pattern area PA to be formed on the surface of the wafer W (see Col. 9, lines 8-21, Fig. 1); and

based on the result of the analysis, correcting the pattern position in the step of pattern exposing on to the surface of the wafer W with the pattern area PA (see Col. 8, lines 25-34, Col. 9, lines 15-20).

Hayashi does not teach explicitly the step of detecting a defect on the surface of the wafer W. Instead, Hayashi teaches the step of detecting a lateral deviation amount caused by a thickness variation between the surface of a reference wafer and the wafer W, and an inclination angle of a chip of the wafer W, which is detected by the horizontal position detecting system 11 (see Col. 7, lines 43-7, Col. 8, lines 55-64, Col. 9, lines 1-14). Here it is understood that the thickness variation causes the surface of the wafer W to be uneven, and thereby affects adversely exposure of the surface of the wafer W with a pattern. Therefore, examiner considers the lateral deviation amount caused by the thickness variation to be a defect of the surface of the wafer W.

With regard to claim 2, Hayashi teaches the pattern forming method as discussed above with respect to claim 1, wherein the position of the pattern area PA is

Art Unit: 2851

corrected such that the lateral deviation amount is not positioned in an edge of the pattern area PA (see Col. 9, lines 15-20; It is understood that the position of the pattern area PA is corrected such that the lateral deviation amount is not positioned in any area of the pattern area PA).

With regard to claim 3, Hayashi teaches the pattern forming method as discussed above with respect to claim 2, wherein the position of the pattern area PA is corrected by shifting the position of the pattern area PA in the x- and/or y-directions (see Col. 9, lines 15-20).

With regard to claims 4-7, Hayashi does not teach explicitly the position of the pattern area PA as discussed above with respect to claim 2 to be corrected with respect to the position of the wafer W by swinging the position of the pattern area PA. Instead, Hayashi teaches the position of the pattern area PA to be corrected with respect to the position of the wafer W by shifting the position of the pattern PA in the x- and/or y-directions for aligning the pattern area PA with the wafer W (see Col. 8, lines 25-45, Col. 9, lines 15-20). However, Hayashi does teach the position of the wafer W to be corrected with respect to the position of the pattern PA by shifting the position of the wafer W in the x- and/or y-directions and by swinging (rotating) the position of the wafer W with respect to the position of the pattern area PA for aligning the wafer W with the pattern area PA (see Col. 4, lines 34-8, Col. 7, lines 63-7). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to correct the position of the pattern area of Hayashi by shifting it in the x- and/or y-

directions and by swinging it by any degree to improve the accuracy of aligning the pattern area PA with the wafer W.

With regard to claim 8, Hayashi teaches the wafer W that is to be exposed as discussed above with respect to claim 2 to be a wafer having a resist film formed thereon (see Col. 4, lines 13-20, 28-38).

With regard to claim 9, Hayashi discloses a pattern forming method in which a main surface of a mask blank (wafer W) used for preparation of a photomask is exposed in a desired pattern (pattern area PA) to form a mask pattern on the mask blank comprising the steps of:

forming position measuring marks on at least two points on a main surface of the mask blank (see Col. 7, lines 22-38);

detecting a lateral deviation amount of the wafer W and obtaining defect analysis data including at least the kind (caused by deviation amount v or thickness variation t) of the lateral deviation amount and the position of the lateral deviation amount relative to the position of the measuring marks (see Col. 7, lines 43-67, Col. 8, lines 25-34, Col. 9, lines 8-20, Fig. 1);

comparing the obtained lateral deviation amount position with the relative position of the pattern area PA that is to be formed on the wafer W so as to select the mask arranging position relative to the wafer W (see Col. 9, lines 15-20); and

measuring the position measuring mark to calculate the light exposure position and applying an exposure treatment to the selected position (see Col. 7, line 20 to Col. 9, line 20).

Hayashi does not teach explicitly the step of detecting a defect on the surface of the wafer W. Instead, Hayashi teaches the step of detecting a lateral deviation amount caused by a thickness variation between the surface of a reference wafer and the wafer W, and an inclination angle of a chip of the wafer W, which is detected by the horizontal position detecting system 11 (see Col. 7, lines 43-7, Col. 8, lines 55-64, Col. 9, lines 1-14). Here it is understood that the thickness variation causes the surface of the wafer W to be uneven, and thereby affects adversely exposure of the surface of the wafer W with a pattern. Therefore, examiner considers the lateral deviation amount caused by the thickness variation to be a defect of the surface of the wafer W.

With regard to claim 10, Hayashi teaches the pattern forming method as discussed above with respect to claim 9, wherein the position of the pattern area PA is corrected such that the lateral deviation amount is not positioned in an edge of the pattern area PA (see Col. 9, lines 15-20; It is understood that the position of the pattern area PA is corrected such that the lateral deviation amount is not positioned in any area of the pattern area PA).

With regard to claim 13, Hayashi teaches the pattern forming method as discussed above with respect to claim 9, wherein the position of the pattern area PA is corrected by shifting the position of the pattern area PA in the x- and/or y-directions (see Col. 9, lines 15-20).

With regard to claims 14-17, Hayashi does not teach explicitly the position of the pattern area PA as discussed above with respect to claim 9 to be corrected with respect to the position of the wafer W by swinging the position of the pattern area PA. Instead,

Hayashi teaches the position of the pattern area PA to be corrected with respect to the position of the wafer W by shifting the position of the pattern PA in the x- and/or y-directions for aligning the pattern area PA with the wafer W (see Col. 8, lines 25-45, Col. 9, lines 15-20). However, Hayashi does teach the position of the wafer W to be corrected with respect to the position of the pattern PA by shifting the position of the wafer W in the x- and/or y-directions and by swinging (rotating) the position of the wafer W with respect to the position of the pattern area PA for aligning the wafer W with the pattern area PA (see Col. 4, lines 34-8, Col. 7, lines 63-7). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to correct the position of the pattern area of Hayashi by shifting it in the x- and/or y-directions and by swinging it by any degree to improve the accuracy of aligning the pattern area PA with the wafer W.

With regard to claim 18, Hayashi discloses an exposure apparatus comprising:

- means (illumination light IL) for exposing a substrate surface (surface of wafer W) with a desired pattern (pattern area PA of reticle R) (see Fig. 1);
- means (horizontal position detecting system 11) for detecting a lateral deviation amount of the wafer W (see Col. 7, lines 43-7, Col. 9, lines 8-14, Fig. 1);
- means (main controller 10) for analyzing the mutual positional relationship between the lateral deviation detected by the horizontal position detecting system 11 and the pattern area PA that is to be formed on the surface of the wafer W (see Col. 9, lines 8-21, Fig. 1); and

means (main controller 10, actuator unit 13) for correcting the position of the pattern area PA in the step of exposing the surface of the wafer W with the pattern based on the result of the analysis (see Col. 8, lines 25-34, Col. 9, lines 15-20).

Hayashi does not teach explicitly means for detecting a defect on the surface of the wafer W. Instead, Hayashi teaches means for detecting a lateral deviation amount caused by a thickness variation between the surface of a reference wafer and the wafer W, and an inclination angle of a chip of the wafer W, which is detected by the horizontal position detecting system 11 (see Col. 7, lines 43-7, Col. 8, lines 55-64, Col. 9, lines 1-14). Here it is understood that the thickness variation causes the surface of the wafer W to be uneven, and thereby affects adversely exposure of the surface of the wafer W with a pattern. Therefore, examiner considers the lateral deviation amount caused by the thickness variation to be a defect of the surface of the wafer W.

With regard to claim 19, Hayashi teaches the exposure apparatus as discussed above with respect to claim 18, wherein:

the horizontal position detecting system 11 includes a laser light source (light source 11a) and a defect detector (photo sensitive element 11) (see Fig. 1);

the main controller 10 consists of a defect detecting-defect position calculating section (see Col. 9, lines 8-20);

the means for correcting the position of the pattern area PA in the step of exposing the surface of the wafer W with the pattern consists of a pattern arrangement shift treating section (see Col. 9, lines 15-20, Fig. 1).

With regard to claim 20, Hayashi teaches the main controller 10 as discussed above with respect to claim 19 to perform at least one of shifting of the position of the pattern area PA in an x- and/or y-directions and a swinging of the pattern area PA position (see Col. 9, lines 15-20).

Allowable Subject Matter

5. Claims 11 and 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
6. The following is a statement of reasons for the indication of allowable subject matter:

With regard to claim 11, the prior art does not teach in combination with all other limitations recited in the claim wherein a pattern arranging position is selected such that a black type defect is buried in a light shielding film pattern, and a white type defect is exposed to a pattern opening that is not covered with the light shielding pattern as set forth in the claim.

With regard to claim 12, the prior art does not teach in combination with all other limitations recited in the claim wherein a pattern arranging position is selected such that a defect lowering the reflectivity is buried in a non-reflecting pattern, and a reflection defect is positioned on an opening that is not covered with a light shielding film pattern as set forth in the claim.

Conclusion

7. The following art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 6,381,873 to Peremychtchev et al.

U.S. Patent No. 6,526,164 to Mansfield et al.

U.S. Patent No. 6,504,609 to Nara et al.

U.S. Patent No. 5,539,514 to Shishido et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Nguyen whose telephone number is 703-305-2771. The examiner can normally be reached on M-F 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Russ Adams can be reached on 703-308-2847. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4900.

mpn
March 6, 2003



RUSSELL ADAMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800